EE 434

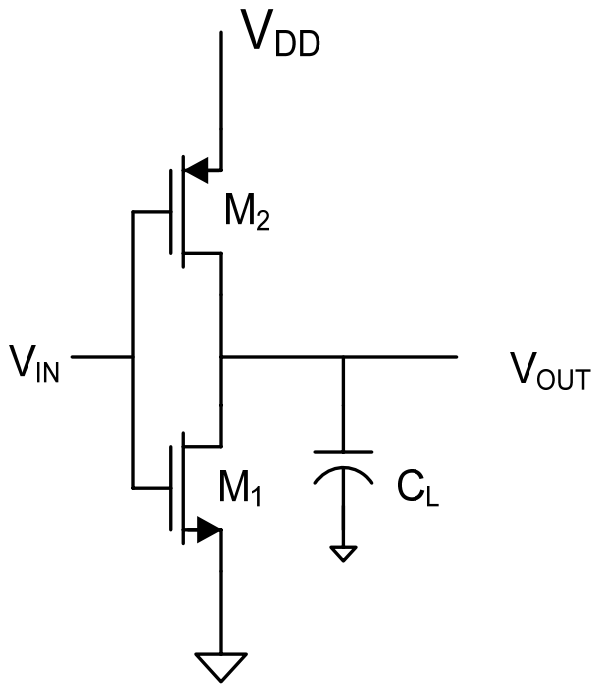
Lecture 35

~~Device Sizing~~

Propagation Delay in Logic Circuits

Review from last time

Device Sizing



Sizing Strategies

- Minimum Size
- Fixed V_{TRIP}
- Equal rise-fall times
  (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance

4 design variables $\{W_1, W_2, L_1, L_2\}$

Invariably will select $L_1 = L_2 = L_{MIN}$

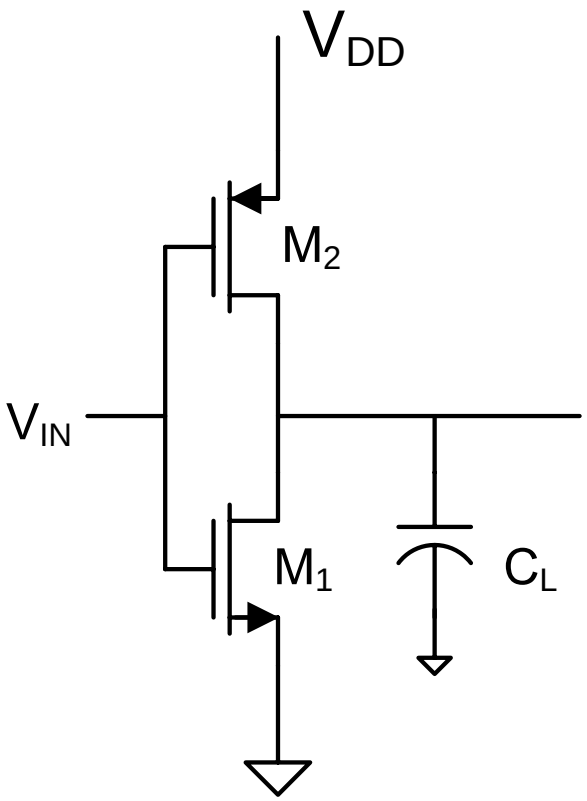
2 degrees of freedom $\{W_1, W_2\}$

Review from last time

Device Sizing

Equal Rise/Fall Device Sizing Strategy
-- (same as $V_{TRIP}=V_{DD}/2$ in typical process considered in example)

Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$



$W_n=W_{MIN}$, $W_p=3W_n$

$$C_{IN}=C_{OX}\left(W_{MIN}L_{MIN}+3W_{MIN}L_{MIN}\right)=4C_{OX}W_{MIN}L_{MIN}$$

$$t_{HL}=t_{LH}=\frac{1}{R_{PD}C_L}$$

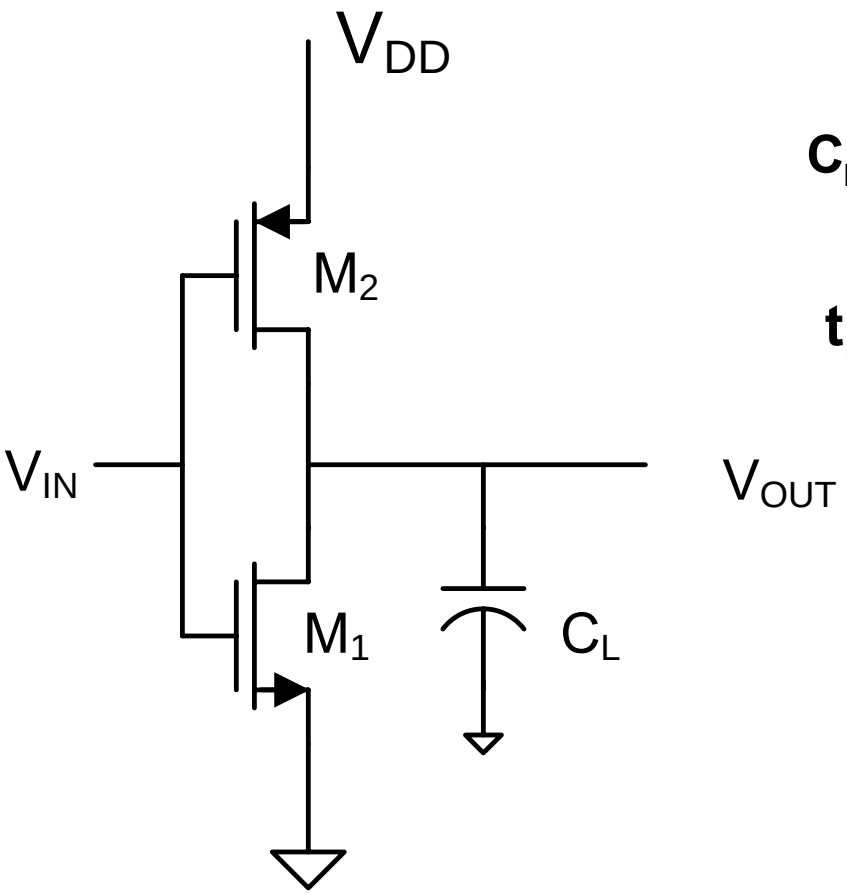
$$t_{PROP}=t_{HL}+t_{LH}=\frac{2}{R_{PD}C_L}$$

Review from last time

Device Sizing

The reference inverter

Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$ $W_n=W_{MIN}$, $W_p=3W_n$



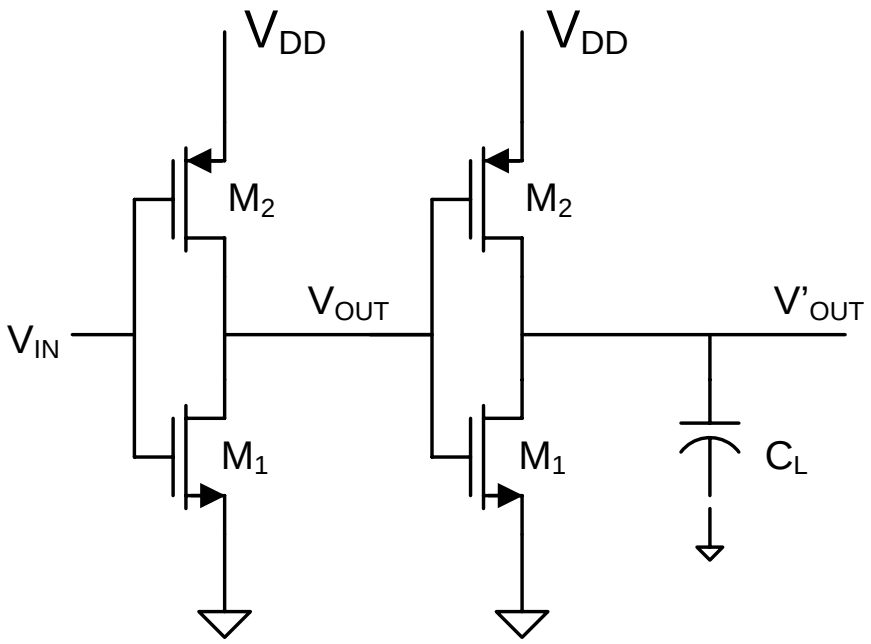
$$C_{REF}=C_{IN}=4C_{OX}W_{MIN}L_{MIN}$$

$$t_{PROP}=t_{HL}+t_{LH}=\frac{2}{R_{PD}C_L}$$

Review from last time

Device Sizing

The reference inverter pair Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$ $W_n=W_{MIN}$, $W_p=3W_n$



$$C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$C_{L1} = C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD}-V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$t_{REF} = t_{HLREF} + t_{LHREF} = \frac{2}{R_{PDREF}C_{REF}}$$

$$C_{IN} = C_{REF} = 4C_{OX}W_{MIN}L_{MIN}$$

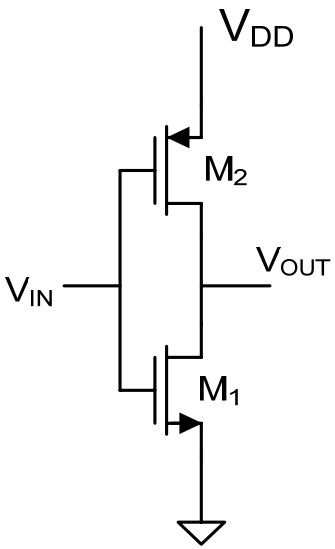
Review from last time

Device Sizing

Equal Rise/Fall Device Sizing Strategy

-- (same as $V_{TRIP}=V_{DD}/2$ in typical process considered in example)

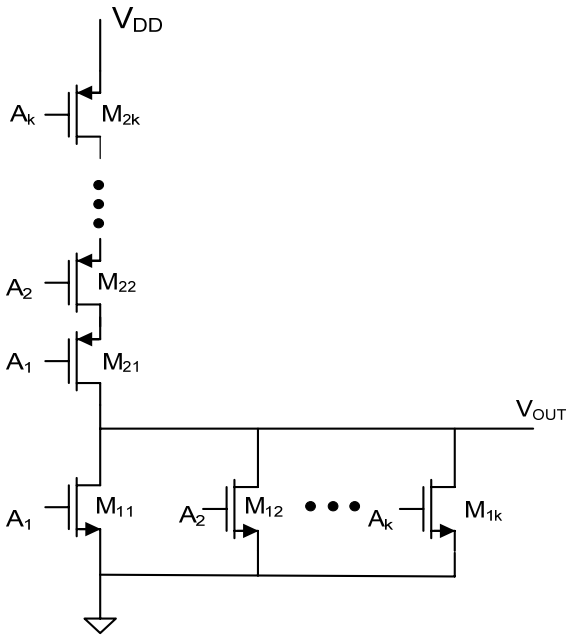
Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$



INV

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

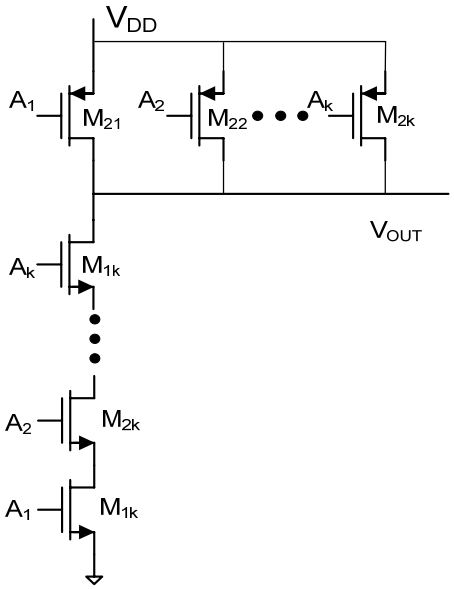
$C_{IN}=C_{REF}$



k-input NOR

$W_n=W_{MIN}$, $W_p=3kW_{MIN}$

$C_{IN}=\left(\frac{3k+1}{4}\right)C_{REF}$



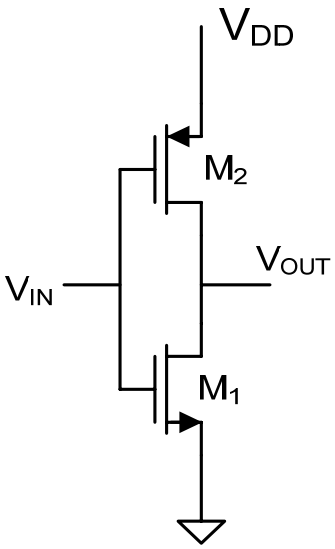
k-input NAND

$W_n=kW_{MIN}$, $W_p=3W_{MIN}$

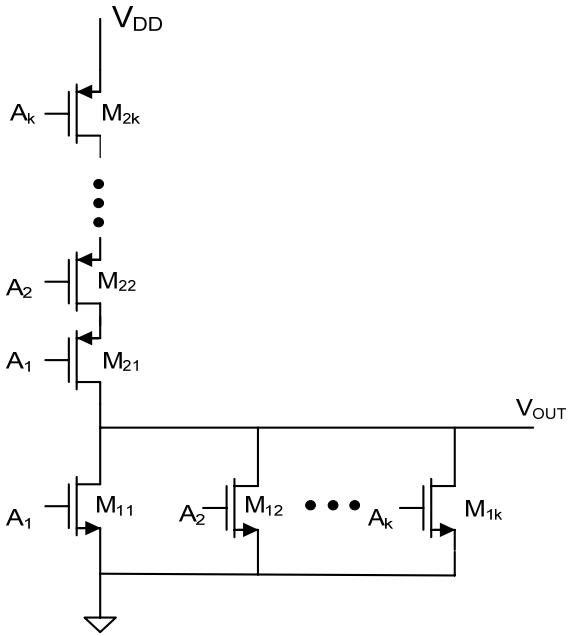
$C_{IN}=\left(\frac{3+k}{4}\right)C_{REF}$

Review from last time

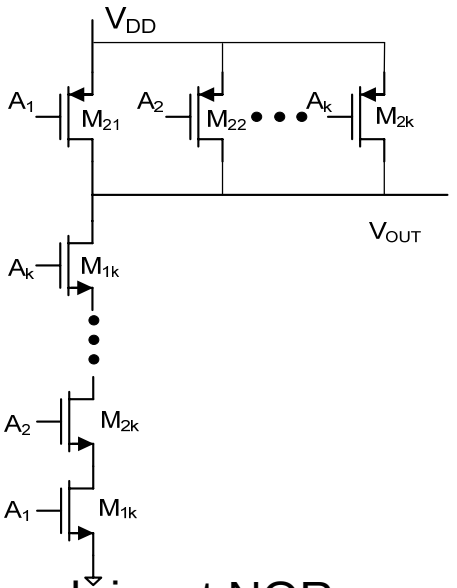
Device Sizing



INV



k-input NOR



k-input NOR

C_{IN} for N_{AND} gates is considerably smaller than for NOR gates for equal worst-case rise and fall times

C_{IN} for minimuim-sized structures is independent of number of inputs and much smaller than CIN for the equal rise/fall time case

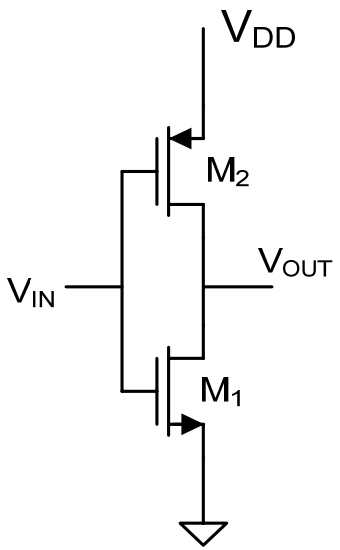
$\frac{C_{REF}}{2}$

or P_{pd}

R_{PU} gets very large for minimum-sized NOR gate

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy : Express delays in terms of those of reference inverter



$$C_{REF} = C_{IN} = 4C_{OX}W_{MIN}L_{MIN}$$

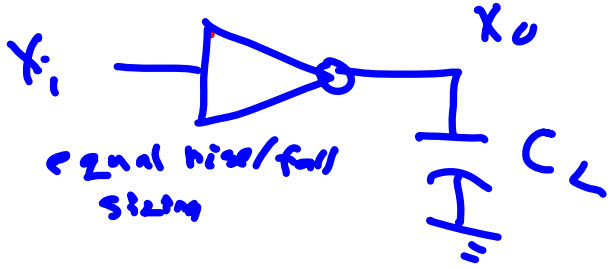
$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD} - V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$t_{REF} = t_{HLREF} + t_{LHREF} = \frac{2}{R_{PDREF} C_{REF}}$$

Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



$$F_{IL} = \frac{C_L}{C_{REF}}$$

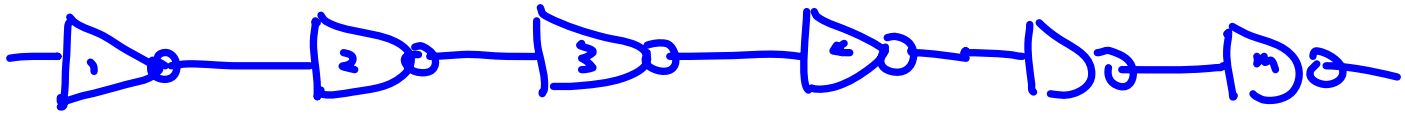
$$t_{HL} = R_{PD} C_L = (R_{PD} C_{REF}) F_{IL}$$

$$t_{LH} = t_{HL}$$

$$t_{PROP} = t_{HL} + t_{LH} = 2 R_{PD} C_{REF} F_{IL}$$

$$t_{PROP} = (t_{REF}) F_{IL}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



Assume m is even

$$t_{HL} = t_{LHm} + t_{HLm-1} + t_{LHm-2} + \cdots + t_{HL_1}$$

$$t_{LH} = t_{HLm} + t_{LHm-1} + \cdots + t_{LH_1}$$

$\therefore$

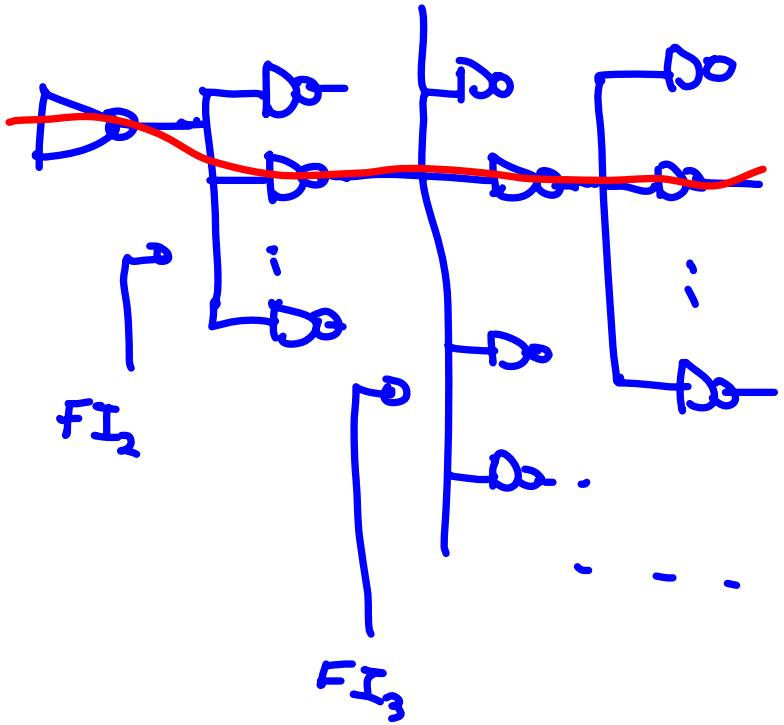
$$t_{PROP} = t_{HL} + t_{LH} = (t_{LHm} + t_{HLm}) + (t_{LH_{m-1}} + t_{HL_{m-1}}) + \cdots + t_{HL_1} + t_{LH_1}$$

$$t_{PROP} = \sum_{i=1}^{m} t_{PROP_i}$$

If m stages are identical & all reference inverters,

$$t_{PROP} = m t_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

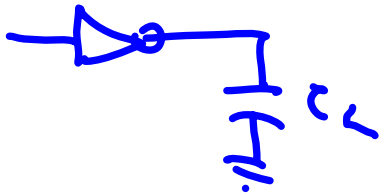


$$t_{PROP} = (t_{REF} \cdot FI_2) + t_{REF} \cdot FI_3 + \cdots + t_{REF} FI_m$$

$$t_{PROP} = \sum_{i=1}^{m} t_{REF} \cdot FI_i$$

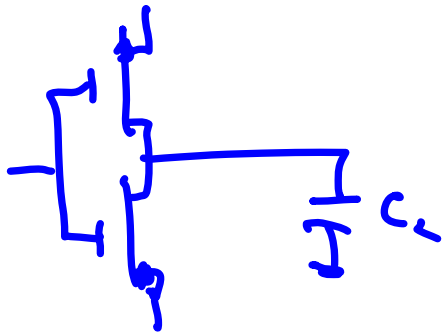
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive (assume equal rise/fall)



$C_L = 10^4 C_{REF}$ ($\sim 20\,pF$)

$t_{PROP} = t_{REF} \cdot F_{IL} = 10^4 t_{REF}$



$R_{pd} = \frac{R_{pDREF}}{k}$

$\therefore t_{PROP} = R_{pd} C_L = \frac{1}{k}(R_{pDREF} C_L) = \frac{t_{REF}}{k}$

$w_n = k\,w_{min}$

$w_p = 3k\,w_{min}$

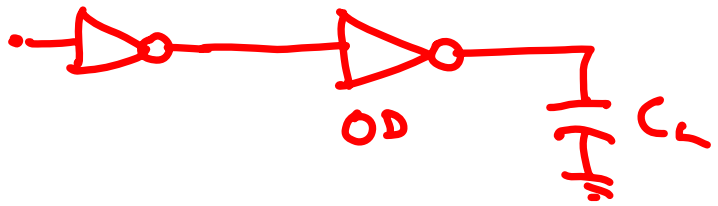
if $k = 10^4$, $t_{PROP} = t_{REF}/10^4 = t_{REF}$

OD = factor by which the widths are increased

beyond those of ref inverter

Propagation Delay in Multiple-Levels of Logic with Stage Loading

an OD factor of k will decrease the delay by a factor of k !



but: may have a problem driving the inverter with a large OD

$$t_{PROP} = t_{REF} \cdot FI_2 + \frac{t_{REF}}{OD} \cdot FI$$

IF $FI = 10^4$

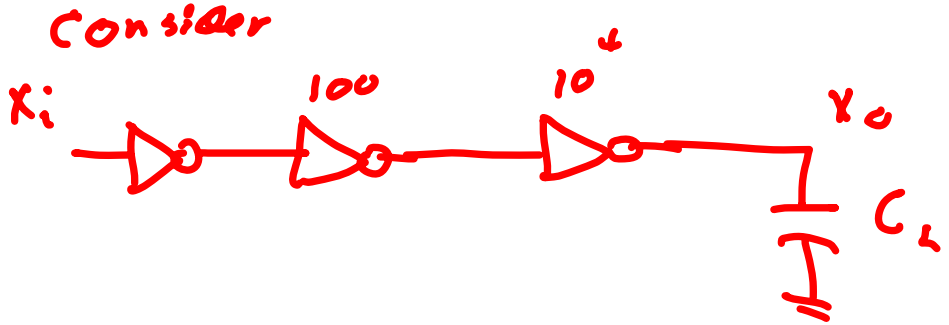
$OD = 10^4$

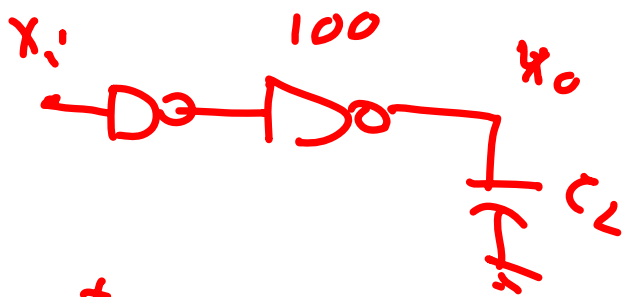
$$= 10^4 t_{REF} + t_{REF}$$

$$= t_{REF}(1 + 10^4)$$

slight increase in prop. delay

Propagation Delay in Multiple-Levels of Logic with Stage Loading





$t_{PROP} = 200\, t_{REF}$

$t_{PROP} = t_1 + t_2 + t_3$

$= (t_{REF})FI_2 + \frac{t_{REF}\, 10^4}{10^2} + t_{REF}\frac{FI_3}{OD_3}$

$= t_{REF}(100 + 100 + 1)$

$t_{PROP} = 201\, t_{REF}$ decrease from $10^4\, t_{REF}$

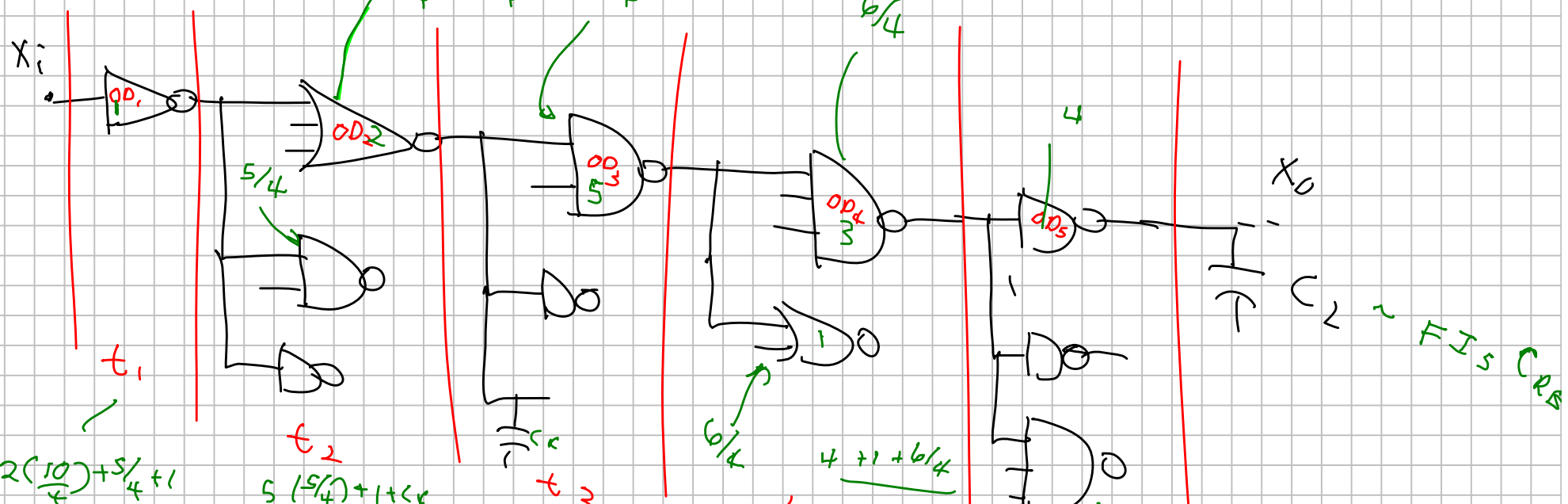
Dramatic Reduction in prop. delay

OD can speed up logic if appropriately used

Propagation Delay in Multiple-Levels of Logic with Stage Loading

- What is the optimal way to drive a given load C_L?
  - How many stages?
  - How much OD on each stage
- Extremely big W/L ratios caused when very large OD
  - but almost always justifiable when speed limitations are present

Logic with varying OD, multiple levels



t_1

$\frac{2\left(\frac{10}{4}\right)+\frac{5}{4}+1}{1}$

t_2

$\frac{5\left(\frac{5}{4}\right)+1+C_R}{2}$ C_{REF}

t_3

$\frac{18/4+6/4}{5}$

t_4 $\frac{4+1+6/4}{3}$

t_5 $\frac{FI_5}{4}$ $6/4$

$$t_{PROP} = t_1 + t_2 + t_3 + t_4 + t_5$$

$$= t_{REF}\frac{FI_2}{OD_1} + t_{REF}\cdot\frac{FI_3}{OD_2} + t_{REF}\frac{FI_4}{OD_3} + \cdots$$

$$\boxed{t_{PROP} = t_{REF}\sum_{i=1}^{m}\frac{FI_{i+1}}{OD_i}}$$

Elmore Delay

OD sizing for NAND & NOR Gates.

- For an OD of h on a NAND or NOR Gate (assuming equal rise/fall times)
  - scale all widths by h